IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant: Philippe Meunier-Beillard et al.
Application No.: 10/586,810
Filed: July 21, 2006
For: METHOD FOR FABRICATING
A MONO-CRYSTALLINE EMITTER

Group Art Unit: 2891
Examiner: Slutsker, Julia
Confirmation No.: 8780

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37(a)

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner dated April 22, 2010, which finally rejected claims 1-20 in the above-identified application. The Office date of receipt of Appellant's Notice of Appeal was July 14, 2010. This Appeal Brief is hereby submitted pursuant to 37 C.F.R. § 41.37(a).

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Date:_____ Signed:_____
Typed Name: Mark A. Wilson

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the full interest in the invention, NXP B.V., of Eindhoven, Netherlands.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.

III. STATUS OF CLAIMS

No claims are withdrawn.

No claims are objected to.

Claims 1-20 stand rejected as follows:

Claims 1-2, 4-5, 8-9, 11-12, 15, and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Oda et al. (U.S. Pat. No. 6,482,710, hereinafter Oda) in view of Sato et al. (U.S. Pat. Pub. No. 2004/0056274 A1, hereinafter Sato).

Claims 3, 10, and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Oda and Sato, and further in view of Koshimizu et al. (U.S. Pat. Pub. No. 2005/0181569 A1, hereinafter Koshimizu).

Claims 6, 13, and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Oda and Sato, and further in view of Verma et al. (U.S. Pat. Pub. No. 2005/0079678 A1, hereinafter Verma).

Claims 7, 14, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Oda and Sato, and further in view of Frei et al. (U.S. Pat. No. 6,509,242 B2, hereinafter Frei).

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Oda and Sato, and further in view of Asai et al. (U.S. Pat. No. 6,455,364 B1, hereinafter Asai).

Claims 1-20 are the subject of this appeal. A copy of the claims is set forth in the Claims Appendix.

IV. STATUS OF AMENDMENTS

There were proposed amendments submitted subsequent to the Final Office Action mailed April 22, 2010. The Advisory Action, received from the Examiner with a notification date of June 23, 2010, stated that the proposed amendments would be entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This section of this Appeal Brief is set forth to comply with the requirements of 37 C.F.R. § 41.37(c)(1)(v) and is not intended to limit the scope of the claims in any way. Examples of implementations of the limitations of independent claims 1, 8, and 15 are described below.

The language of claim 1 relates to a method for growing a mono-crystalline emitter for a bipolar transistor. The method includes providing a trench formed on a silicon substrate having opposed silicon oxide side walls. Fig. 1, trench 14, silicon substrate 16, silicon oxide sidewalls 12; Detailed Description, page 2, line 32 through page 3, line 1. The method also includes selectively growing a highly doped first mono-crystalline layer on the silicon substrate in the trench. Fig. 1, highly doped first mono-crystalline layer 18; Detailed Description, page 3, lines 1-13. The method also includes forming an amorphous or polysilicon layer over the silicon oxide side walls. Fig. 2, amorphous or polysilicon layer 21; Detailed Description, page 4, lines 17-19. The method also includes forming a second mono-crystalline layer over the first mono-crystalline layer. Fig. 2, second mono-crystalline layer 22; Detailed Description, page 4, lines 21-22. Claim 1 further recites wherein the amorphous or polysilicon layer and the second mono-crystalline layer are formed by non-selectively growing a second silicon layer over the trench. Fig. 2, second silicon layer 20; Detailed Description, page 4, lines 16-24.

The language of claim 8 relates to a method for forming a highly n-type doped layer in a semiconductor wafer. The method includes providing a first active region comprised of a silicon substrate. Fig. 1, silicon substrate 16; Detailed Description, page 2, line 32 through page 3, line 1. The method also includes providing a second region

comprised of silicon oxide. Fig. 1, silicon oxide 12; Detailed Description, page 2, line 32 through page 3, line 1. The method also includes selectively growing a highly doped first mono-crystalline layer on the silicon substrate. Fig. 1, highly doped first mono-crystalline layer 18; Detailed Description, page 3, lines 1-13. The method also includes forming an amorphous or polysilicon layer over the silicon oxide. Fig. 2, amorphous or polysilicon layer 21; Detailed Description, page 4, lines 17-19. The method also includes forming a second mono-crystalline layer over the highly doped mono-crystalline layer. Fig. 2, second mono-crystalline layer 22; Detailed Description, page 4, lines 21-22. Claim 1 further recites wherein the amorphous or polysilicon layer and the second mono-crystalline layer are formed by non-selectively growing a second silicon layer over the first active region and the second region. Fig. 2, second silicon layer 20; Detailed Description, page 4, lines 16-24.

The language of claim 15 relates to a method for growing a mono-crystalline emitter for a bipolar transistor. The method includes providing a trench formed on a substrate having opposed silicon oxide side walls. Fig. 1, trench 14, substrate 16, silicon oxide sidewalls 12; Detailed Description, page 2, line 32 through page 3, line 1. The method also includes growing a highly doped layer on the substrate in the trench using selective epitaxial growth. Fig. 1, highly doped layer 18; Detailed Description, page 3, line 4 through page 4, line 15. The method also includes forming an amorphous or polysilicon layer over the silicon oxide side walls. Fig. 2, amorphous or polysilicon layer 21; Detailed Description, page 4, lines 17-19. The method also includes forming a mono-crystalline layer over the highly doped layer. Fig. 2, mono-crystalline layer 22; Detailed Description, page 4, lines 21-22. Claim 1 further recites wherein the amorphous or polysilicon layer and the second mono-crystalline layer are formed by growing a second layer over the trench using differential epitaxial growth. Fig. 2, second layer 20; Detailed Description, page 4, lines 16-33.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1-2, 4-5, 8-9, 11-12, 15, and 17 are patentable over the combination of Oda and Sato under 35 U.S.C. § 103(a).

B. Whether claims 3, 10, and 16 are patentable over the combination of Oda, Sato, and Koshimizu under 35 U.S.C. § 103(a).

C. Whether claims 6, 13, and 18 are patentable over the combination of Oda, Sato, and Verma under 35 U.S.C. § 103(a).

D. Whether claims 7, 14, and 19 are patentable over the combination of Oda, Sato, and Frei under 35 U.S.C. § 103(a).

E. Whether claim 20 is patentable over the combination of Oda, Sato, and Asai under 35 U.S.C. § 103(a).

VII. ARGUMENT

For the purposes of this appeal, claims 1-2, 4-5, 8-9, 11-12, 15, and 17 are argued together as a group for purposes of the question of patentability over the combination of Oda and Sato under 35 U.S.C. § 103(a). Claims 3, 10, and 16 are argued together as a separate group for purposes of the question of patentability over the combination of Oda, Sato, and Koshimizu under 35 U.S.C. § 103(a). Claims 6, 13, and 18 are argued together as a separate group for purposes of the question of patentability over the combination of Oda, Sato, and Verma under 35 U.S.C. § 103(a). Claims 7, 14, and 19 are argued together as a separate group for purposes of the question of patentability over the combination of Oda, Sato, and Frei under 35 U.S.C. § 103(a). Claim 20 is argued separately for the purpose of the question of patentability over the combination of Oda, Sato, and Asai under 35 U.S.C. § 103(a).

A. Claims 1-2, 4-5, 8-9, 11-12, 15, and 17 are patentable over the combination of Oda and Sato

Appellants respectfully submit that claim 1 is patentable over the combination of Oda and Sato because the cited references do not teach all of the limitations of the claim. Claim 1 recites:

> "A method for growing a mono-crystalline emitter for a bipolar transistor, comprising:

providing a trench formed on a silicon substrate having opposed silicon oxide side walls;

selectively growing a highly doped first mono-crystalline layer on the silicon substrate in the trench;

forming an amorphous or polysilicon layer over the silicon oxide side walls; and

forming a second mono-crystalline layer over the first mono-crystalline layer;

wherein the amorphous or polysilicon layer and the second mono-crystalline layer are formed by non-selectively growing a second silicon layer over the trench" (emphasis added).

Oda and Sato do not teach all of the limitations of claim 1. In particular, Oda and Sato do not teach "selectively growing a highly doped first mono-crystalline layer," "forming a polysilicon layer over the silicon oxide side walls" and "forming a second mono-crystalline layer over the first mono-crystalline layer" by "non-selectively growing a second silicon layer over the trench," as recited in claim 1. The Final Office Action recites the p-type layer 13 of Oda as teaching the step of selectively growing a highly doped first mono-crystalline layer (Final Office Action, page 3. See Oda, Fig. 4C). The Final Office Action further recites the emitter polysilicon electrode 19 grown over the silicon oxide isolation layer 11 of Oda (see Oda, Fig. 5C) as teaching the step of forming a polysilicon layer over the silicon oxide side walls. The Final Office Action then recites the intrinsic base layer 14 of Oda as teaching the step of forming a second mono-crystalline layer. However, claim 1 recites that the amorphous or polysilicon layer and the second mono-crystalline layer are formed by growing a second silicon layer.

In contrast to claim 1, Oda does not teach that both a second mono-crystalline layer and a polycrystalline layer are formed by growing a single layer. Rather, Oda teaches that the intrinsic base layer 14 is formed in an opening of a multilayer film (Oda, col. 7, lines 39-43 and Fig. 5A) and then an emitter electrode 19 made of polysilicon is deposited over the p-type intrinsic base layer 14 (Oda, col. 7, lines 48-51 and Fig. 5C). However, the p-type intrinsic base layer 14 and the emitter electrode 19 of Oda are not formed by growing the same layer, but are formed in two different steps by growing two separate layers. Therefore, Oda does not teach "forming a polysilicon layer over the silicon oxide sidewalls [...] wherein the amorphous or polysilicon layer and the second mono-crystalline layer are formed by [...] growing a second silicon layer over the trench", as recited in claim 1 (emphasis added).

The Final Office Action admits that Oda does not teach that "the second mono-crystalline layer [is] formed by non-selectively growing a second silicon layer" (emphasis added) and the Final Office Action recites the non-selectively grown SiGe film 9 of Sato as teaching the missing limitation of Oda (Final Office Action, page 3. See Sato, Fig. 5E).

Appellants respectfully submit that the proposed combination of cited references is improper because Oda teaches away from replacing the intrinsic base layer 14 of Oda with the SiGe film 9 of Sato. Within the context of a rejection under 35 U.S.C. § 103, MPEP 2141 recognizes three factual inquiries that should be analyzed:

1. Determine the scope and content of the prior art;
2. Ascertain the differences between the claimed invention and the prior art; and
3. Resolve the level of ordinary skill in the art.

In ascertaining the differences between the claimed invention and the prior art (factual inquiry #2), the MPEP further states that "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." MPEP 2141.02(VI) (emphasis in original) (citing *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). The MPEP also recognizes that "the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." Id. (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). Thus, the description of a mere alternative embodiment is not necessarily a teaching away if the alternative embodiment is not criticized, discredited, or otherwise discouraged. Conversely, the Federal Circuit explained "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference..." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 132y (Fed. Cir. 2009) (emphasis added) (quoting *Ricoh Co., Ltd. v. Quanta Computer Inc.*, 550 F.3d 1325, 1332 (Fed. Cir. 2008) (further quoting *In*

re Kahn, 441 F.3d 977, 990 (Fed. Cir. 2006))). Thus, a reference teaches away if it discourages the teaching.

In the present case, Oda teaches away from the proposed combination of Oda and Sato because Oda discourages the use of non-selectively growing a silicon film over the trench to form a polycrystalline layer over silicon oxide side walls, as taught by Sato. Specifically, Oda teaches that epitaxial growth conditions are such that the intrinsic base layer 14 is selectively grown only in the trench and no polycrystalline layer is deposited on the silicon oxide isolation layers 11 (Oda, Fig. 5A and col. 6, lines 20-27). Oda discourages the use of growth conditions of the intrinsic base layer 14 where a polycrystalline layer would be deposited on the silicon oxide isolation layers 11 (Oda, col. 10, lines 15-26). Therefore, the proposed combination of Oda and Sato is improper because Oda teaches away from non-selectively growing a silicon film over the trench to form a polycrystalline layer over the silicon oxide side walls. Accordingly, Appellants respectfully assert that the rejection of claim 1 is improper because Oda teaches away from the proposed combinations of cited references.

Furthermore, Appellants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness for the independent claim 1 because the Examiner has provided mere conclusory statements and/or failed to provide some articulated reasoning with some rational underpinning in support of the obviousness rejections. In order to establish a *prima facie* rejection of a claim under 35 U.S.C. 103, the Examiner must present a clear articulation of the reason why the claimed invention would have been obvious. MPEP 2142 (citing *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398 (2007)). The analysis must be made explicit. Id. Additionally, rejections based on obviousness cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. Id.

> Examiner has failed to provide an articulated reasoning with a rational underpinning to support the legal conclusion of obviousness with respect to modifying the teachings of Oda with the teachings of Sato

On page 3 of the Final Action of April 22, 2010, the Examiner admits that Oda does not teach that "the second mono-crystalline layer is formed by non-selectively growing a second silicon layer over the trench" However, the Examiner alleges on page 3 of the Final Office Action that Sato teaches these limitations. The Examiner then alleges on page 3 of the Final Office Action that it would have been obvious to modify Oda with Sato "for the purpose of improving transistor characteristics."

Thus, the Examiner has provided the following statement in support of an obviousness rejection of claim 1 with respect to modifying the teachings of Oda with the teachings of Sato: "for the purpose of improving transistor characteristics." However, this statement is a mere conclusory statement, which cannot sustain an obvious rejection. Even if this statement is correct, the Examiner has only provided a statement regarding an end result of the modification, not an articulated reasoning why it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device described in Oda using the teaching of Sato. Appellants also note herein that the use of the phrase "improving transistor characteristics" (emphasis added) without any factual support regarding how the resulting transistor characteristics would be improved indicates that the Examiner's statement is merely a conclusory statement.

Even if the Examiner's statement is not a mere conclusory statement, the Examiner has failed to provide an articulated reasoning with a rational underpinning to support the legal conclusion of obviousness with respect to modifying the teachings of Oda with the teachings of Sato, as required by the MPEP and *KSR*. The purpose alleged by the Examiner indicates that the Examiner's rationale in support of the obviousness rejection is that there is some teaching, suggestion, or motivation that would have led one of ordinary skill to combine the cited references' teachings to arrive at the claimed invention. For such rationale, MPEP §2143 (G) and the applicable case law require the following:

> "To reject a claim based on this rationale, Office personnel must resolve the *Graham* factual inquiries. Then, Office personnel must articulate the following:

(1) a finding that there was some teaching, suggestion, or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;
(2) a finding that there was reasonable expectation of success; and
(3) whatever additional findings based on the *Graham* factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

... If any of these findings cannot be made, then this rationale cannot be used to support a conclusion that the claim would have been obvious to one of ordinary skill in the art." (emphasis added).

If the Appellants' assumption of the Examiner's rationale as described above is correct, then the Appellants are entitled to have the foregoing required items articulated. If the Examiner's rejection is based on some other rationale, Appellants are entitled to know what that rationale is and to be given an opportunity to respond. "The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness." MPEP §2142.

For the reasons presented above, Oda and Sato, alone or in combination, do not teach all of the limitations of claim 1 because Oda and Sato do not teach "selectively growing a highly doped first mono-crystalline layer," "forming a polysilicon layer over the silicon oxide side walls" and "forming a second mono-crystalline layer over the first mono-crystalline layer" by "non-selectively growing a second silicon layer over the trench," as recited in claim 1. Furthermore, the proposed combination of Oda and Sato is improper because the proposed combination would render the primary reference inoperable for its intended purpose. Furthermore, Oda teaches away from non-selectively growing a second silicon layer over the trench to form a polysilicon layer over the silicon oxide side walls. Accordingly, Appellants respectfully assert that claim 1 is patentable over Oda and Sato, because Oda and Sato do not teach all of the limitations of claim 1 and because the proposed combination of Oda and Sato is improper and, hence, is insufficient to establish a *prima facie* case of obviousness.

Independent Claims 8 and 15

Independent claims 8 and 15 include similar limitations to claim 1. Although the language of claims 8 and 15 differs from the language of claim 1 and the scope of claims 8 and 15 should be interpreted independently of claim 1, Appellants respectfully assert that the remarks provided above in regard to claim 1 apply also to claims 8 and 15.

Dependent Claims 2, 4-5, 9, 11-12, and 17

Claims 2 and 4-5 are dependent on claim 1, claims 9 and 12-14 are dependent on claim 8, and claim 17 is dependent on claim 15. Appellants respectfully assert that claims 2, 4-5, 9, 11-12, and 17 are allowable at least based on allowable base claims. Additionally, each of claims 2, 4-5, 9, 11-12, and 17 may be allowable for further reasons.

B. Claims 3, 10, and 16 are patentable over the combination of Oda, Sato, and Koshimizu

Claim 3 is dependent on independent claim 1. Claim 10 is dependent on independent claim 8. Claim 16 is dependent on independent claim 15. Appellants respectfully submit that dependent claims 3, 10, and 16 are patentable over the cited references at least based on an allowable base claim. Additionally, claims 3, 10, and 16 may be allowable for further reasons.

C. Claims 6, 13, and 18 are patentable over the combination of Oda, Sato, and Verma

Claim 6 is dependent on independent claim 1. Claim 13 is dependent on independent claim 8. Claim 18 is dependent on independent claim 15. Appellants respectfully submit that dependent claims 6, 13, and 18 are patentable over the cited references based on an allowable base claim. Additionally, claims 6, 13, and 18 may be allowable for further reasons.

D. Claims 7, 14, and 19 are patentable over the combination of Oda, Sato, and Frei

Claim 7 is dependent on independent claim 1. Claim 14 is dependent on independent claim 8. Claim 19 is dependent on independent claim 15. Appellants respectfully submit that dependent claims 7, 14, and 19 are patentable over the cited references at least based on an allowable base claim. Additionally, claims 7, 14, and 19 may be allowable for further reasons.

E. Claim 20 is patentable over the combination of Oda, Sato, and Asai

Claim 20 is dependent on independent claim 15. Appellants respectfully submit that dependent claim 20 is patentable over the cited references at least based on an allowable base claim. Additionally, claim 20 may be allowable for further reasons.

VIII. CONCLUSION

For the reasons stated above, claims 1-20 are patentable over the cited references. Thus, the rejections of claims 1-20 should be withdrawn. Appellants respectfully request that the Board reverse the rejections of claims 1-20 under 35 U.S.C. § 103(a) and, since there are no remaining grounds of rejection to be overcome, direct the Examiner to enter a Notice of Allowance for claims 1-20.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/mark a. wilson/

Date: September 14, 2010

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IX. CLAIMS APPENDIX

1. A method for growing a mono-crystalline emitter for a bipolar transistor, comprising:

providing a trench formed on a silicon substrate having opposed silicon oxide side walls;

selectively growing a highly doped first mono-crystalline layer on the silicon substrate in the trench;

forming an amorphous or polysilicon layer over the silicon oxide side walls; and

forming a second mono-crystalline layer over the first mono-crystalline layer;

wherein the amorphous or polysilicon layer and the second mono-crystalline layer are formed by non-selectively growing a second silicon layer over the trench.

2. The method of claim 1, wherein the step of selectively growing a highly doped first mono-crystalline layer is accomplished using selective epitaxial growth.

3. The method of claim 2, wherein the selective epitaxial growth using a precursor selected from the group consisting of: SiH_2Cl_2, SiH_4, $SiCl_4$, $SiCl_3$, $Si2H_6$, Si_3H_8, GeH_4, and SiH_3CH_3.

4. The method of claim 1, wherein the step of non-selectively growing the second silicon layer is accomplished using differential epitaxial growth.

5. The method of claim 1, wherein the first mono-crystalline layer is substantially grown only on an active area on the silicon substrate.

6. The method of claim 1, comprising the further step of performing a salicidation process using a silicide selected from the group consisting of: titanium, cobalt and nickel.

7. The method of claim 1, wherein the mono-crystalline emitter is n-type doped with an element selected from the group consisting of: phosphorous and arsenic.

8. A method for forming a highly n-type doped layer in a semiconductor wafer,

comprising:

providing a first active region comprised of a silicon substrate;

providing a second region comprised of silicon oxide;

selectively growing a highly doped first mono-crystalline layer on the silicon substrate;

forming an amorphous or polysilicon layer over the silicon oxide; and

forming a second mono-crystalline layer over the highly doped mono-crystalline layer;

wherein the amorphous or polysilicon layer and the second mono-crystalline layer are formed by non-selectively growing a second silicon layer over the first active region and the second region.

9. The method of claim 8, wherein the step of selectively growing a highly doped first mono-crystalline layer is accomplished using selective epitaxial growth.

10. The method of claim 8, wherein the selective epitaxial growth uses a precursor selected from the group consisting of: SiH_2Cl_2 and SiH_4, $SiCl_4$, $SiCl_3$, $Si2H_6$, Si_3H_8, GeH_4, and SiH_3CH_3.

11. The method of claim 8, wherein the step of non-selectively growing the second silicon layer is accomplished using differential epitaxial growth.

12. The method of claim 8, wherein the first mono-crystalline layer is substantially grown only on the active region.

13. The method of claim 8, comprising the further step of performing a salicidation process using a silicide selected from the group consisting of: titanium, cobalt and nickel.

14. The method of claim 8, wherein the highly n-type doped layer is doped with an element selected from the group consisting of: phosphorous and arsenic.

15. A method for growing a mono-crystalline emitter for a bipolar transistor, comprising:

providing a trench formed on a substrate having opposed silicon oxide side walls;

growing a highly doped layer on the substrate in the trench using selective epitaxial growth;

forming an amorphous or polysilicon layer over the silicon oxide side walls; and

forming a mono-crystalline layer over the highly doped layer;

wherein the amorphous or polysilicon layer and the second mono-crystalline layer are formed by growing a second layer over the trench using differential epitaxial growth.

16. The method of claim 15, wherein the selective epitaxial growth using a precursor selected from the group consisting of: SiH_2Cl_2, SiH_4, $SiCl_4$, $SiCl_3$, $Si2H_6$, Si_3H_8, GeH_4, and SiH_3CH_3.

17. The method of claim 15, wherein the highly doped layer comprises a mono-crystalline layer that is substantially grown only on an active area on the substrate.

18. The method of claim 15, comprising the further step of performing a salicidation process using a silicide selected from the group consisting of: titanium, cobalt and nickel.

19. The method of claim 15, wherein the mono-crystalline emitter is n-type doped with an element selected from the group consisting of: phosphorous and arsenic.

20. The method of claim 15, wherein the mono-crystalline emitter is p-type doped using boron.

X. EVIDENCE APPENDIX

There is no evidence submitted with this Appeal Brief.

XI. RELATED PROCEEDINGS APPENDIX

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.